



# DCR5900A28

# **Phase Control Thyristor**

DS6151-2 September 2014 (LN31946)

### FEATURES

- Double Side Cooling
- High Surge Capability

#### **KEY PARAMETERS**

V <sub>DRM</sub>	2800V
I <sub>T(AV)</sub>	5900A
I <sub>TSM</sub>	79000A
dV/dt*	2000V/µs
dl/dt	250A/µs

#### \* Higher dV/dt selections available

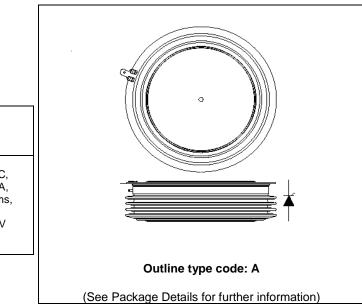


Fig. 1 Package outline

#### **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

#### **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR5900A28 DCR5900A26 DCR5900A24	2800 2600 2400	$\begin{array}{l} T_{vj} = -40^{\circ}\text{C} \text{ to } 125^{\circ}\text{C},\\ I_{DRM} = I_{RRM} = 300\text{mA},\\ V_{DRM}, V_{RRM} t_p = 10\text{ms},\\ V_{DSM} \& V_{RSM} = \\ V_{DRM} \& V_{RRM} + 100V\\ \text{respectively} \end{array}$

Lower voltage grades available.

#### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR5900A26

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.



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### **CURRENT RATINGS**

T<sub>case</sub> = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Sid	de Cooled			
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	5900	А
I <sub>T(RMS)</sub>	RMS value	-	9277	А
Ι <sub>Τ</sub>	Continuous (direct) on-state current	-	7715	А

## SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}C$	79.0	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	V <sub>R</sub> = 0	31.2	MA <sup>2</sup> s

## THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	DC	-	0.00603	°C/W
		Single side cooled	Anode DC	-	0.01024	°C/W
			Cathode DC	-	0.01467	°C/W
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
$T_{vj}$	Virtual junction temperature	Blocking V <sub>DRM</sub> / V <sub>RRM</sub>		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
F <sub>m</sub>	Clamping force			74.0	91.0	kN

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# **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	300	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, ga	ate open	-	2000	V/µs
dl/dt	Rate of rise of on-state current	From 67% $V_{\text{DRM}}$ to 2x $I_{\text{T}(\text{AV})}$	Repetitive 50Hz	-	250	A/µs
		Gate source 30V, $10\Omega$ ,	Non-repetitive	-	500	A/µs
		t <sub>r</sub> < 0.5µs, T <sub>j</sub> = 125°C				
V <sub>T(TO)</sub>	Threshold voltage – Low level	500 to 4000A at T <sub>case</sub> = 125°	С	-	0.766	V
	Threshold voltage – High level	4000 to 8000A at T <sub>case</sub> = 125°C		-	0.92	V
٢ <sub>T</sub>	On-state slope resistance – Low level	500A to 4000A at T <sub>case</sub> = 125°C		-	0.1048	mΩ
	On-state slope resistance – High level	4000A to 8000A at T <sub>case</sub> = 125°C		-	0.06	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, 10 $\Omega$		-	3	μs
		$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$I_T = 5000A, T_j = 125^{\circ}C,$ $V_R = 200V, dI/dt = 5A/\mu s,$			250	μs
		$dV_{DR}/dt = 20V/\mu s linear$				
Qs	Stored charge	- I <sub>T</sub> = 3000A, T <sub>j</sub> = 125°C, dI/dt − 1A/µs, V <sub>Rpeak</sub> ~1700V, V <sub>R</sub> ~ 1100V		1520	3280	μC
I <sub>RR</sub>	Reverse recovery current			32	56	A
١L	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	A
Ι <sub>Η</sub>	Holding current	$T_j = 25^{\circ}C, R_{G-K} = \infty, I_{TM} = 500A, I_T = 5A$		-	300	mA

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# GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V <sub>GT</sub>	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
$V_{GD}$	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	300	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

# CURVES

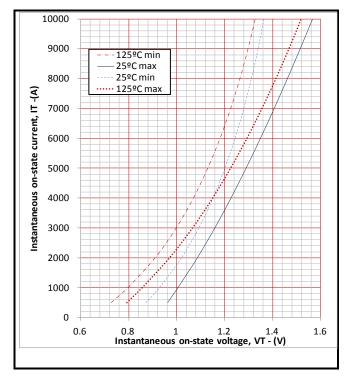


Fig.2 Maximum & minimum on-state characteristics

### **V<sub>TM</sub> EQUATION**

$$V_{TM} = A + BIn (I_T) + C.I_T + D.\sqrt{I_T}$$

Where A = 1.073114 B = -0.098284 C = -0.000016 D = 0.015109 these values are valid for  $T_j$  = 125°C for I<sub>T</sub> 500A to 8000A



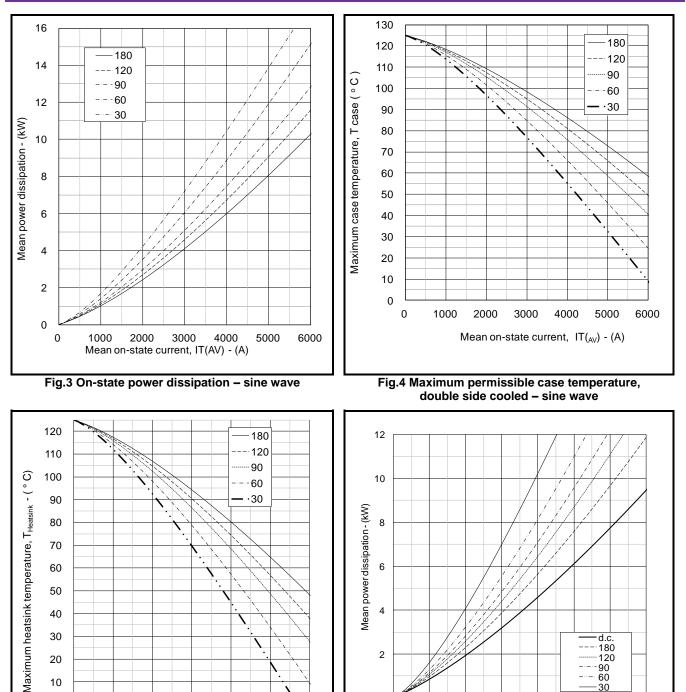


Fig.5 Maximum permissible heatsink temperature, double side cooled - sine wave

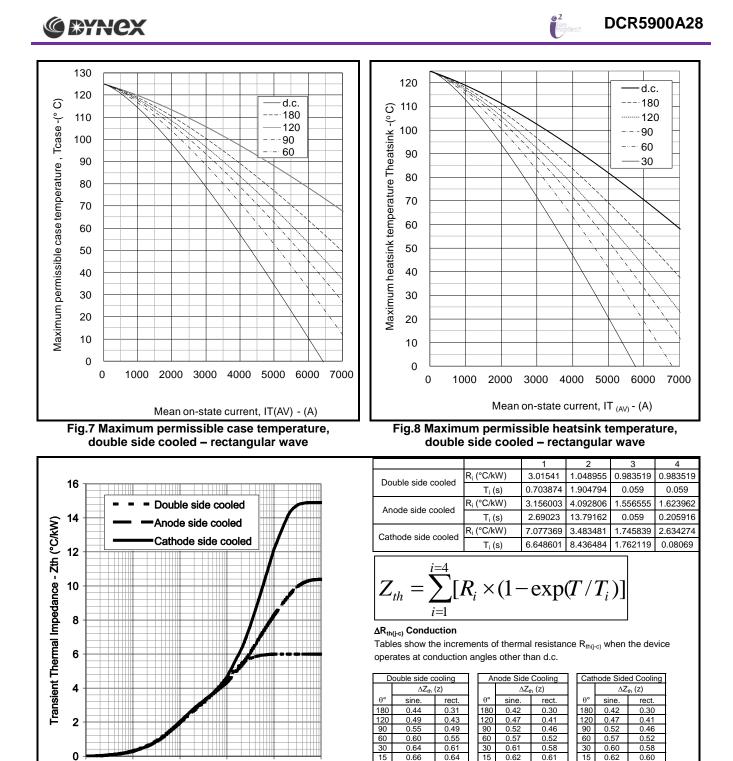
Mean on-state current, IT(AV) - (A)



Mean on-state current, IT (AV) - (A)

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#### Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

0.001

0.01

0.1

1

Time (s)

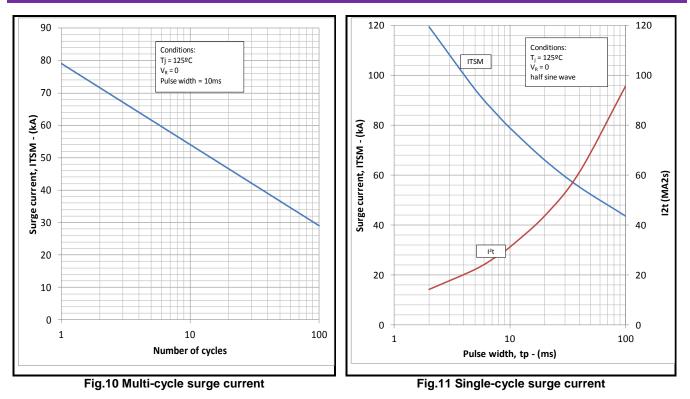
10

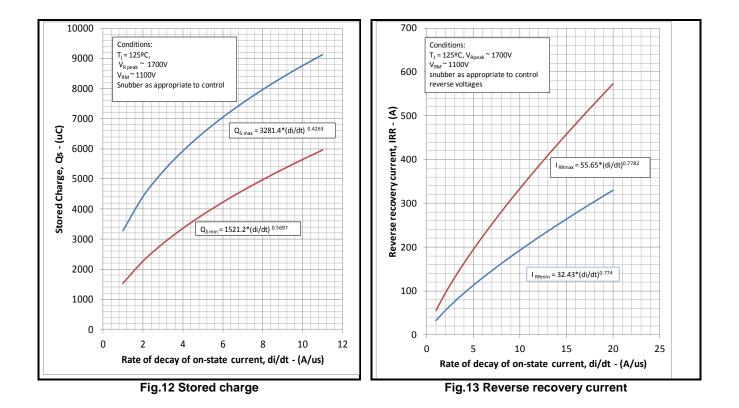
100



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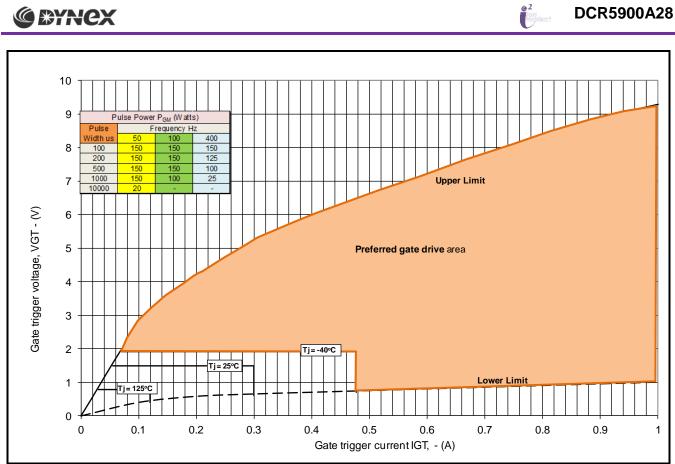


Fig14 Gate Characteristics

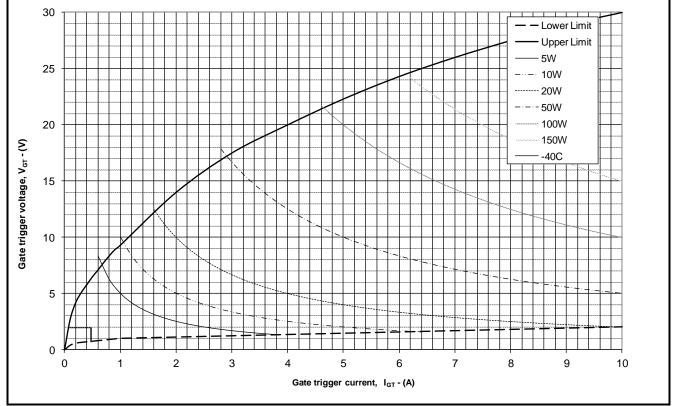


Fig. 15 Gate characteristics



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# PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

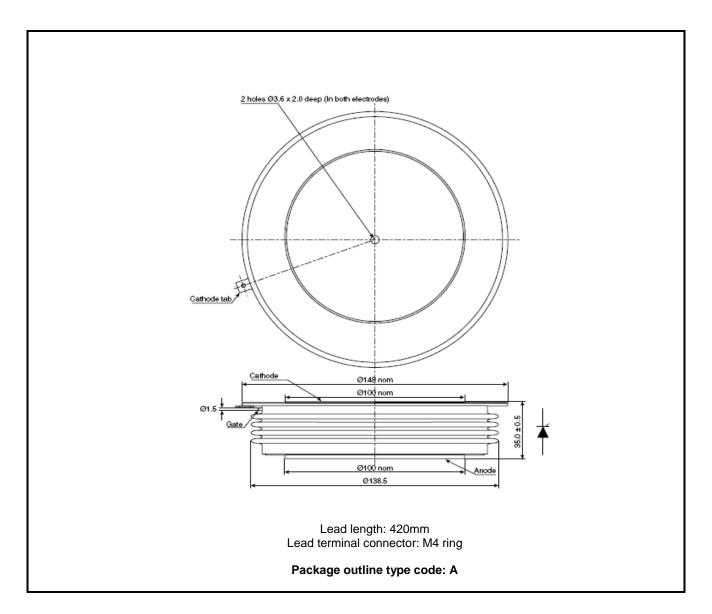


Fig.16 Package outline



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